

Refine Search

Search Results -

Terms	Documents
L2 same select\$3	8

Database:

US Pre-Grant Publication Full-Text Database

US Patents Full-Text Database
 US OCR Full-Text Database
 EPO Abstracts Database
 JPO Abstracts Database
 Derwent World Patents Index
 IBM Technical Disclosure Bulletins

Search:

L3

Search History

DATE: Friday, January 20, 2006 [Printable Copy](#) [Create Case](#)

Set Name Query

side by side

DB=PGPB; PLUR=YES; OP=OR

L3 L2 same select\$3

L2 L1 same (chip or IC or "integrated circuit")

L1 (memory adj1 (card or board)) near10 (USB or "universal serial bus")

Hit Count Set Name

result set

8 L3

71 L2

1181 L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L1 and L4	3

Database:

US Pre-Grant Publication Full-Text Database
 US Patents Full-Text Database
 US OCR Full-Text Database
 EPO Abstracts Database
 JPO Abstracts Database
 Derwent World Patents Index
 IBM Technical Disclosure Bulletins

Search:

L5

Refine Search

Recall Text

Clear

Interrupt

Search History

 DATE: Friday, January 20, 2006 [Printable Copy](#) [Create Case](#)

Set Name Query

side by side

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L5 11 and L4L4 L3 same select\$3L3 L2 same (chip or IC or "integrated circuit")L2 (memory adj1 (card or board)) same (USB or "universal serial bus")L1 439/638,639.ccls.

Hit Count Set Name

result set

3 L519 L4180 L32366 L21023 L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L2 same select\$3	0

Database:

US Pre-Grant Publication Full-Text Database
 US Patents Full-Text Database
 US OCR Full-Text Database
 EPO Abstracts Database
 JPO Abstracts Database
 Derwent World Patents Index
 IBM Technical Disclosure Bulletins

Search:

L5

Search History

DATE: Friday, January 20, 2006 [Printable Copy](#) [Create Case](#)

Set Name Query

side by side

Hit Count Set Name

result set

DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L5 L2 same select\$3

0 L5

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L4 L2 same select\$3

8 L4

DB=PGPB; PLUR=YES; OP=OR

L3 L2 same select\$3

8 L3

L2 L1 same (chip or IC or "integrated circuit")

71 L2

L1 (memory adj 1 (card or board)) near10 (USB or "universal serial bus")

1181 L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(439/59 439/79 439/945 361/684 361/686 361/737 710/300 710/301 710/302 710/303 710/62 710/74 710/313 710/316 711/100 711/103).ccls.	10318

Database:

US Pre-Grant Publication Full-Text Database
 US Patents Full-Text Database
 US OCR Full-Text Database
 EPO Abstracts Database
 JPO Abstracts Database
 Derwent World Patents Index
 IBM Technical Disclosure Bulletins

Search:

L6

Refine Search

Recall Text

Clear

Interrupt

Search History

 DATE: Friday, January 20, 2006 [Printable Copy](#) [Create Case](#)

Set Name Query

side by side

Hit Count Set Name

result set

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L6 710/300-303,62,74,313,316;711/100,103;361/684,686,737;439/59,79,945.ccls. 10318 L6

DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L5 L2 same select\$3 0 L5

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L4 L2 same select\$3 8 L4

DB=PGPB; PLUR=YES; OP=OR

L3 L2 same select\$3 8 L3

L2 L1 same (chip or IC or "integrated circuit") 71 L2

L1 (memory adj1 (card or board)) near10 (USB or "universal serial bus") 1181 L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L2 and L6	13

Database:

US Pre-Grant Publication Full-Text Database
 US Patents Full-Text Database
 US OCR Full-Text Database
 EPO Abstracts Database
 JPO Abstracts Database
 Derwent World Patents Index
 IBM Technical Disclosure Bulletins

Search:

L7

Refine Search

Recall Text

Clear

Interrupt

Search History

 DATE: Friday, January 20, 2006 [Printable Copy](#) [Create Case](#)

Set Name Query

side by side

Hit Count Set Name

result set

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L7 l2 and L6

13

L7L6 710/300-303,62,74,313,316;711/100,103;361/684,686,737;439/59,79,945.ccls.

10318

L6

DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L5 L2 same select\$3

0

L5

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L4 L2 same select\$3

8

L4

DB=PGPB; PLUR=YES; OP=OR

L3 L2 same select\$3

8

L3L2 L1 same (chip or IC or "integrated circuit")

71

L2L1 (memory adj1 (card or board)) near10 (USB or "universal serial bus")

1181

L1

END OF SEARCH HISTORY

EAST - [Untitled1:1]

File View Edit Tools Window Help

☐ Drafts
☐ Pending
☒ **Active**
 L1: (408) (memory adj1
 L2: (32) 11 same (chip
 L3: (1) 12 same select\$
☐ Failed
☐ Saved
☐ Favorites
☐ Tagged (0)
☐ UDC
☐ Queue
☐ Trash

Search List Browse Queue Clear
 DBs USPAT ☒ Plural
 Default operator: OR ☐ Highlight all hit terms initially

BRS form IS&R form Image Text HTML

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comment	Error	Definit	Er
1	BRS	L1	408	(memory adj1 (card or board)) same (USB or	USPA	2006/01/20 10:25				
2	BRS	L2	32	11 same (chip or IC or "integrated circui	USPA	2006/01/20 10:26				
3	BRS	L3	1	12 same select\$3	USPA	2006/01/20 10:26				

	U	1	Document ID	Issue Dat	Pages	Title	Current OR	Current XR
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6916208 B2	20050712	7	Memory card reader for electronic devices	439/639	235/439; 439/638



Welcome United States Patent and Trademark Office

Search Results

[BROWSE](#)[SEARCH](#)[IEEE XPLORE GUIDE](#)[SUPPORT](#)

Results for "((memory card) and (usb or (universal serial bus))<in>metadata)"

Your search matched 3 of 1302021 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

☒ e-mail
 printer friendly

» Search Options

[View Session History](#)[New Search](#)

Modify Search

(((memory card) and (usb or (universal serial bus))<in>metadata)



Check to search only within this results set

» Key

Display Format:



Citation



Citation & Abstract

IEEE JNL IEEE Journal or Magazine

IEEE JNL IEEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEEE Conference Proceeding

IEEE STD IEEE Standard

Select Article Information



1. Memory device packaging - from leadframe packages to wafer level packages

Wei Koh;

High Density Microsystem Design and Packaging and Component Failure Analysis, 2004. HDP '04. Proceeding of the Sixth IEEE CPMT Conference on

30 June-3 July 2004 Page(s):21 - 24

Digital Object Identifier 10.1109/HPD.2004.1346666

[AbstractPlus](#) | Full Text: [PDF](#)(598 KB) IEEE CNF

2. Bad peripherals

Arce, I.;

Security & Privacy Magazine, IEEE

Volume 3, Issue 1, Jan-Feb 2005 Page(s):70 - 73

Digital Object Identifier 10.1109/MSP.2005.6

[AbstractPlus](#) | Full Text: [PDF](#)(448 KB) IEEE JNL

3. System-on-chip design for TV-centric home networks

Qiang Peng; Jin Jing;

Consumer Communications and Networking Conference, 2004. CCNC 2004. First IEEE

5-8 Jan. 2004 Page(s):501 - 506

Digital Object Identifier 10.1109/CCNC.2004.1286912

[AbstractPlus](#) | Full Text: [PDF](#)(1416 KB) IEEE CNF
 Indexed by
[Help](#) [Contact Us](#) [Privacy & Security](#) [IEEE.org](#)

© Copyright 2005 IEEE -- All Rights Reserved



AbstractPlus

View Search Results | Next Article

Access this document

Full Text: PDF (598 KB)

Download this citation

Choose Citation

Download EndNote, ProCite, RefMan

Learn More

Rights & Permissions



Learn More

Phone : Login : Logout : Access Information : Alerts : Sitemap : Help

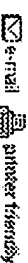
Welcome United States Patent and Trademark Office

BROWSE

SEARCH

IEEE Xplore Guide

SUPPORT



Memory device packaging - from leadframe packages to wafer level packages

Yael Koh

Kingston Technol. Co., Fountain Valley, CA, USA

This paper appears in: **High Density Microsystem Design and Packaging and Component Failure Analysis, 2004, HDP '04, Proceeding of the Sixth IEEE CPMT Conference on**

Publication Date: 30 June-3 July 2004

On page(s): 21 - 24

Number of Pages: 393

ISSN:

INSPEC Accession Number: 8109391

Digital Object Identifier: 10.1109/HDP.2004.1346666

Posted online: 2004-11-01 11:52:34.0

Abstract

The digital revolution has taken the consumer electronics by a storm in just two short years. Portable and handheld electronics devices now have insatiable appetite for digital storage. Hence, **memory cards** in the form of **USB Drive (U-drive)**, **compact flash (CF)**, **secured digital (SD)**, **memory stick**, and **multimedia card (MMC)** are now proliferating in the market. Moreover, the volatile memory dynamic random access memory (DRAM) for PC and notebook computing and gaming are also increasing in density and speed. With all these improvement, the memory device packaging technology is also evolving rapidly, from the traditional leadframe packages to smaller chip scale packages (CSP) and wafer level packages (WLP). This paper will cover the four major topics: (1) Review of the DRAM packages and their applications - DRAM packages are used primarily in the fabrication of DIMM modules that are inserted to the motherboards in PC and notebook computers. With newer DRAM technology in double data rate (DDR) and its second generation, DDR2, to be deployed this year, the clock rate is much higher and the number of I/Os increasing. Packages therefore are changing from the leadframe TSOP type 2 to faster CSPs such as fine pitch BGA (FBGA). (2) Review of the flash **memory card** packages - non-volatile memory flash and SRAM packages are generally smaller and have had lower density of 256Mb and below. But more recently high density (512Mb) and hence larger flash devices are more common. The conventional package TSOP type 1 may become inadequate to meet new performance demands and the form factor for miniaturization. Alternative new packages such as VFBCA CSP are described. (3) Stacking - 3D stacking have now been widely utilized to increase the memory density and saving weight and space. The two main options for stacking - die stack and package stack, each has its own advantages and concerns. The selection criteria and suitable applications for both the DRAM DIMM modules and various flash **memory card** formats are discussed in detail. (4) Future trends and conclusion - the convergence of packaging technology for the computing and consumer electronics is apparent under the same market and technology drivers - form factor miniaturization, lightweight, low profile, high speed, and high performance. Packaging for high-density memory devices is moving toward faster and smaller CSP packages, with the technology and processes for wafer level CSP and wafer level 3D stacking emerging in the horizon.

Index Terms

inspec

Controlled Indexing

fine-pitch technology flash memories memory cards notebook computers random-access storage stacking

Non-controlled Indexing

3D stacking CSP packages DDR2 DRAM DIMM modules DRAM packages SRAM packages USB drive VFBGA
CSP chip scale packages clock rate compact flash computing electronics consumer electronics die stack digital
revolution digital storage double data rate dynamic random access memory fine pitch BGA flash memory card
packages form factor initialization gaming applications handheld electronics devices high-density memory
devices leadframe ISOP type 2 leadframe packages memory cards memory density memory device packaging
memory stick motherboards multimedia card nonvolatile memory flash notebook computing package stack
packaging technology portable electronics devices secured digital volatile memory wafer level CSP wafer level
packages

Author Keywords

Not Available

References

No references available on IEEE Xplore.

Citing Documents

No citing documents available on IEEE Xplore.

4 View Search Results | Next Article ▶



Help Contact Us Privacy & Security IEEE.org

© Copyright 2005 IEEE - All Rights Reserved